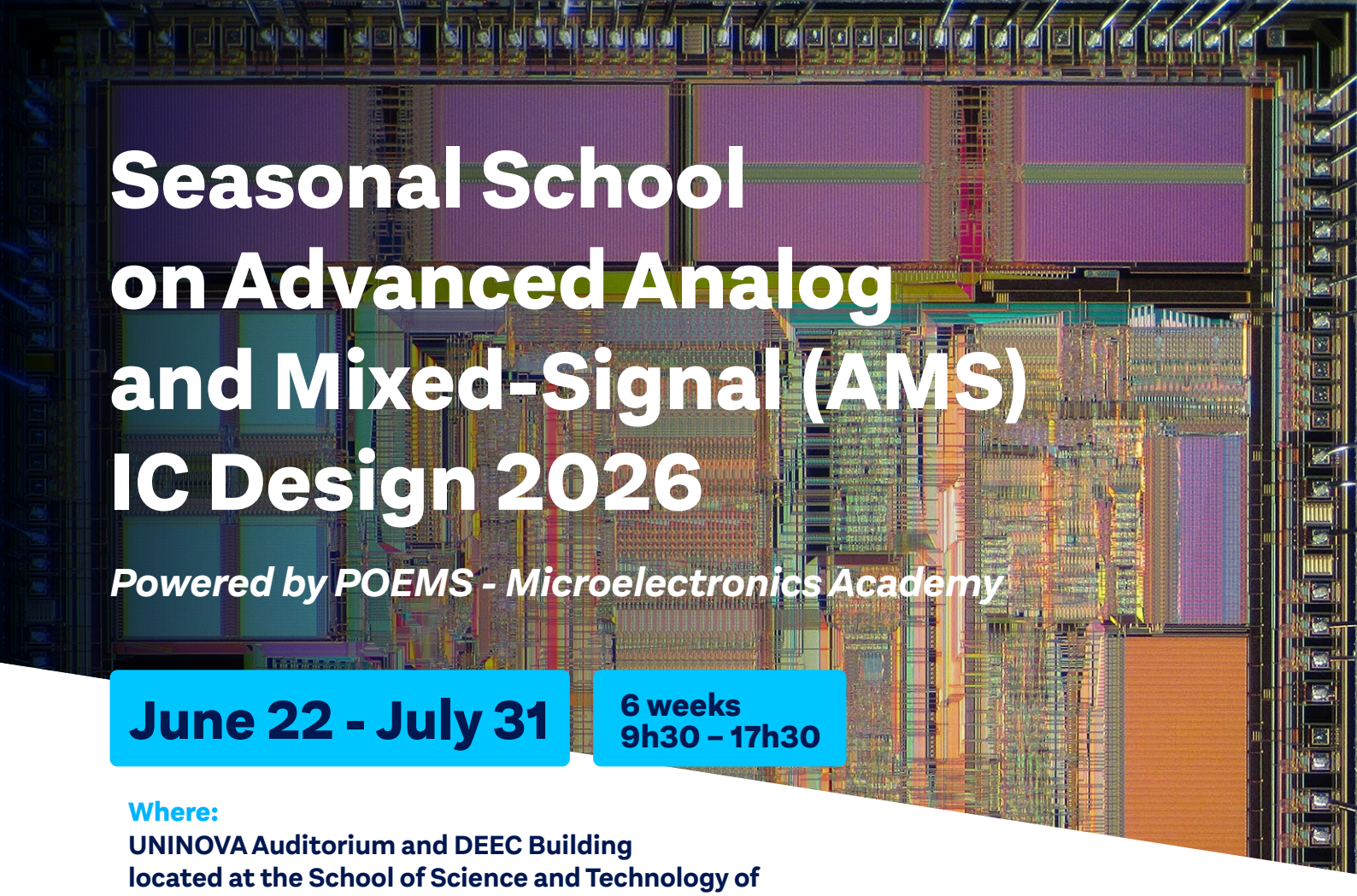


Seasonal School on Advanced Analog and Mixed-Signal (AMS) IC Design 2026

Powered by POEMS - Microelectronics Academy

June 22 - July 31

6 weeks
9h30 – 17h30

Where:
UNINOVA Auditorium and DEEC Building located at the School of Science and Technology of NOVA University of Lisbon (NOVA FCT)

Apply and register now for a **FREE** Seasonal School on Advanced AMS IC Design, in Lisbon, at UNINOVA and benefit from this unique opportunity.

Participation in the Seasonal School may be accredited with up to 6 ECTS through microcredentials issued by NOVA School of Science and Technology.

Apply until Jun 7, 17h00 WEST

URL for registration link:
https://forms.gle/V9TtU2zjpioLeurM9

Registration link:

Target Audience:
Mainly MSc and PhD students and early-career professionals in electrical and computer engineering – will engage with best practices in design-for-yield (DFY) and design-for-manufacturing (DFM).

Program:
This intensive course is a key initiative of POEMS, strongly committed to promoting advanced training in AMS IC design with a particular emphasis on state-of-the-art CMOS technologies. The program offers an immersive, hands-on learning experience focused on the design of complex AMS building blocks, targeting applications in automotive, IoT, and wireless/wireline communications.
Kick-off Day (FREE and OPEN to ALL): June 22, 10h00 – 17h00, UNINOVA Auditorium

Technical Sponsors:

Broadcast Technology/ Circuits and Systems/ Consumer Technology Joint Chapter

Solid-State Circuits Chapter

Keynote Speakers June 22

José Franca

Instituto Superior Técnico, Universidade de Lisboa; Former CEO of CHIPIDEA
Portugal

"Opening Speech"
June 22

José Franca graduated in Electrical Engineering from Instituto Superior Técnico (1978), received the Ph.D. from Imperial College London (1985), and completed the executive program on Management of Research and Technology-based Innovation at the Sloan School of Management, MIT (1992). He is Professor at Instituto Superior Técnico. In 1997 José Franca co-founded and became CEO and Chairman of Chipidea Microelectronics which pioneered and became a worldwide leader in the Semiconductor Analog Mixed-Signal IP industry until his departure in 2008 upon the acquisition by MIPS Technologies. Currently with c. 700 engineers in Portugal, the former Chipidea operation is now the largest European engineering centre of Synopsys. In 2012 José Franca was appointed by the Government of Portugal Chairman of the Board and CEO of Portugal Ventures, which he served until 2015 with the mandate to establish a modern, internationally recognized technology-based entrepreneurial ecosystem in Portugal laying out solid foundations for the attraction of international venture capital and steady worldwide inflows of talent and experience.

Tiago L. Costa

Delft University of Technology
The Netherlands

"Integrated Circuits Enabling the Next Generation of Chronic Brain Therapies"
June 22

Tiago L. Costa is an Associate Professor at the Department of Microelectronics at Delft University of Technology, The Netherlands, where he leads the Therapeutic Ultrasound Microsystems Lab. Dr. Costa received his PhD in Electrical and Computer Engineering from Instituto Superior Técnico in Lisbon, Portugal, in 2015, after which he joined Columbia University, NY, as a postdoctoral researcher, where he worked on ultrasound phased arrays for non-invasive neural stimulation and wireless power transfer for implantable medical devices. Since moving to TU Delft in 2019, his group has been advancing programmable ultrasound microsystems that incorporate integrated circuits and microfabricated materials to develop innovative ultrasound technologies for therapeutic applications.

Lou Hutter

CEO of Lou Hutter Consulting LLC
USA

"The World of Analog Semiconductor Technology"
June 22

Lou Hutter received an S.M. degree in electrical engineering from the Massachusetts Institute of Technology (MIT), Cambridge, MA, USA, in 1978, focusing on solid-state physics. He spent 29 years at Texas Instruments (TI) until retiring in 2007, where he was responsible for worldwide Analog CMOS, BCD, and RF-SiGe silicon technology development, design enablement, production ramps, and technology transfers that supported every business unit in the company. He was elected a TI Fellow (top 1%) in 1995. In 2008, he joined DB HiTek, in Seoul, S. Korea, as Senior Vice President and General Manager of the newly created Analog Foundry. During his tenure there, he established DB HiTek as a leading Analog/BCD specialty foundry. Since 2012, he is the CEO of Lou Hutter Consulting LLC, assisting foundries, IDMs, fabless design houses, and others in the areas of analog/power roadmaps and technology optimization, design enablement, organizational management, and business development. Lou has 50+ U.S. patents, has published over 35 journal articles, has co-authored 1 book entitled *Silicon Analog Components*, now in its 2nd edition, as well as a newly released 5-book series entitled *Silicon Components and Processes Self Study*. He resides in Lisbon, Portugal.

Jiawei Xu

Laboratory of Analog and Mixed-Signal VLSI (AMSV), University of Macau
China

"Brain-Inspired Computing Architecture and Energy-Efficient AI Chips"
June 22

Jiawei Xu received the B.S. degree in electronic engineering and the Ph.D. degree in microelectronics from Fudan University, Shanghai, China, in 2016 and 2022, respectively. From 2022 to 2024, she was a Postdoctoral Researcher with the School of Electrical Engineering and Computer Science at KTH Royal Institute of Technology, Stockholm, Sweden. She is currently an Assistant Professor with the State Key Laboratory of Analog and Mixed-Signal VLSI (AMSV), University of Macau.

Her research interests include brain-inspired chip design, neuromorphic computing architectures, deep compression of AI models, and neural network accelerators. She has authored and co-authored over 30 publications in international journals and conferences, including ICLR, IEEE TCAS-I/II, TBioCAS, and TII. She actively serves the academic community as a Technical Program Committee (TPC) member for DATE (2025–2026) and AICAS (2026), and served as the Industrial Papers Chair for ICTA 2025.

João de Melo

Brookhaven National Laboratory (BNL)
USA

"Wafer-Scale Stitched Sensor Chips for Next-Generation Silicon Tracking Detectors"
June 22

João de Melo received his B.Sc. and M.Sc. degrees in Electrical and Computer Engineering from NOVA University of Lisbon (FCT-UNL) in 2008 and 2010, and his Ph.D. in 2017, focusing on continuous-time sigma-delta modulators (CTΔΣMs).

He was a researcher at UNINOVA (2015–2016), contributing to the European PROTEUS project on low-power ΔΣMs for IoT. In 2016, he joined S3 Semiconductors (later ADESTO Technologies and DIALOG Semiconductors), working as a technical lead on CTΔΣMs. In 2020, he joined CERN, contributing to radiation-tolerant particle detectors and readout ASICs, including MAPS.

Since 2023, he has been a Staff Scientist at Brookhaven National Laboratory (BNL), working on the silicon vertex detector for the Electron-Ion Collider (EIC). He serves as Co-convener of Work Package 1 on MAPS development within the Silicon Vertex Tracker (SVT). He also collaborates on the ALICE ITS3 upgrade at CERN. His research interests include energy-efficient ΔΣMs, high-speed SerDes, and radiation-tolerant particle detectors.

Seasonal School Instructors' List:

José Franca

Full Professor at IST/University of Lisbon; founder and CEO of CHIPIDEA; former CEO of Portugal Ventures

João Goes

Full Professor at NOVA FCT; former Project Manager at CHIPIDEA; co-founder and CTO of ACACIA SEMI

José-Maria Moniz

C-suite Executive at ARM; former Global Vice President of Sales at Cosmic Circuits; former Vice President of Sales and Customer Service at CHIPIDEA

Paulo Santos

Principal Engineer at POWER TOOLS; former Senior Engineer at SILICON LABS, Austin, TX

Edgar Albuquerque

Principal Engineer at PETsys

Michael Figueredo

Senior member of Technical Staff at AURA Semiconductor Co., Ltd

Luís B. Oliveira

Associate Professor at NOVA FCT

João P. Oliveira

Associate Professor at NOVA FCT; co-founder of KOALA TECH

Hugo Serra

Assistant Professor at NOVA FCT

Nuno Paulino

Associate Professor at NOVA FCT; former Analog Design Engineer at ROCKWELL Semiconductor, Irvine, CA; co-founder ACACIA SEMI

Rui Tavares

Assistant Professor at NOVA FCT

Sónia Gonçalves

Director of the Digital Team at SYNOPSYS; former Senior Engineer at CHIPIDEA

André Costa

Manager of the Digital Implementation Team at SYNOPSYS

Benjamin Tardivel

Analog Design Manager at RENESAS Portugal

Marco Rodrigues

Analog Design Assistant Manager at RENESAS Portugal

Marcelo Dal Alba

Staff Analog Design Engineer at RENESAS Portugal

Helder Santos

Staff Analog Design Engineer at RENESAS Portugal

Seasonal School Instructors' List (cont.):

Blazej Nowacki

Staff Analog Design Engineer at RENESAS Portugal

Filipe Viegas

Senior Analog Design Engineer at RENESAS Portugal

Miguel Castilho

Senior Analog Design Engineer at RENESAS Portugal

Fábio Vidago

Analog Design Engineer at RENESAS Portugal

Hugo Pinto

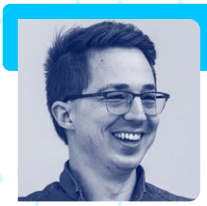
Analog Design Engineer at RENESAS Portugal

Tristan Cakebread

IC Design Engineer at the Analogue IC Team, Science and Technologie Facilities Council (STFC) - Microelectronics Support Centre (MSC), UK

Rowan Read

IC Design Engineer at the Analogue IC Team, Science and Technologie Facilities Council (STFC) - Microelectronics Support Centre (MSC), UK



Thomas Seccombe

IC Design Engineer at the Analogue IC Team, Science and Technologie Facilities Council (STFC) - Microelectronics Support Centre (MSC), UK

Tom Whitford

IC Design Engineer at the Analogue IC Team, Science and Technologie Facilities Council (STFC) - Microelectronics Support Centre (MSC), UK

William Burbidge

IC Design Engineer at the Analogue IC Team, Science and Technologie Facilities Council (STFC) - Microelectronics Support Centre (MSC), UK

Detailed Program

Seasonal School on Advanced AMS IC Frontend Design

June 22	Opening Day
June 23	**RENESAS:** Technology Characterization, PVT Variations & Monte Carlo
June 24–25	**RENESAS & UNINOVA:** Comparator Circuits
June 26	**RENESAS:** ADCs Modelling and Performance Parameters
June 29 – July 1	**ARM & START2SCALE:** Semiconductor Entrepreneurship Module (Part I)
July 2 – 3	**RENESAS:** SAR ADCs
July 6 – 8	**RENESAS & UNINOVA:** Pipeline ADCs & Residue Amplifiers
July 9 – 10	**PETsys & POWERTOOLS:** Bandgap Voltage References
July 13 – 15	**ARM & START2SCALE:** Semiconductor Entrepreneurship Module (Part II)
July 16 – 17	**PETsys & AURASEMI & POWERTOOLS:** Voltage Regulators (LDOs)
July 20 – 24	**SYNOPSYS:** Digital Design: Simulation, Implementation & Verification
July 27 – 31	**EUROPRACTICE** Course: Advanced Node Advanced Analogue IC Design

POWERTOOLS TECHNOLOGIES · UK Research and Innovation · Science and Technology Facilities Council · EUROPRACTICE · PETsys Electronics

START2SCALE · RENESAS · SYNOPSYS · Aurasemi