Winter School on Analog and Mixed-Signal (AMS) Layout IC Design 2026

January 26 - February 11

3 WEEKS **09h30 - 17h30**

Registration Link:

SCAN ME

URL for registration Link:
https://forms.gle/NQ7ATVq2YvtL8ptPA

WHERE:

Laboratories 3.7 and 3.8, located at DEEC Building, at the School of Science and Technology of NOVA University of Lisbon (NOVA FCT)

Apply and register now for a FREE in presence Winter School, in Lisbon, at UNINOVA and benefit from this unique opportunity.

Apply until January 25, 17h00 WEST

TARGET AUDIENCE:

Mainly BSc and MSc students in Electrical and Computer Engineering and Physics Engineering

PROGRAM:

This intensive course is a key initiative of POEMS, strongly committed to promoting advanced training in AMS IC frontend and backend design, with a particular emphasis on state-of-the-art CMOS technologies and other emerging technologies.
The program offers an immersive, hands-on learning experience focused on the layout design of complex AMS building blocks, targeting applications in automotive, IoT, and wireless/wireline communications.

Kick-off Morning (OPEN to ALL): January 26, 10h00 – 12h00, UNINOVA Auditorium

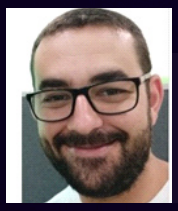
Technical Sponsors:

UNINOVA Instituto de Desenvolvimento de Novas Tecnologias
NOVA Faculdade de Ciências e Tecnologia
POEMS Portuguese Competence Centre in Semiconductors
CTS
IEEE Portugal Section
fct Fundação para a Ciência e a Tecnologia
BTS IEEE Broadcast Technology Society
CAS
IEEE CTSoc Consumer Technology Society
Broadcast Technology/ Circuits and Systems/ Consumer Technology Joint Chapter
SSCS IEEE Solid-State Circuits Society
Solid-State Circuits Chapter
SYNOPSYS
RENESAS
POWERTOOLS TECHNOLOGIES
Funded by the European Union

INSTRUCTORS LIST:

ENG. NUNO PENETRA

Analog Design Assistant Manager at RENESAS Portugal



ENG. MSc. DIOGO CRUZ-DIAS

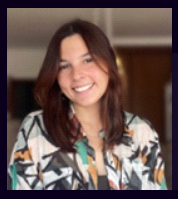
Senior Layout Engineer at RENESAS Portugal

ENG. MSc. DUARTE BATISTA

Senior Layout Engineer at RENESAS Portugal

ENG. MSc. RITA SIMÕES

Senior Layout Design Engineer at Synopsys



ENG. MSc. MARIANA BARROSINHO

Currently PhD student at NOVA FCT

ENG. MSc. DIMO NAYDENOV

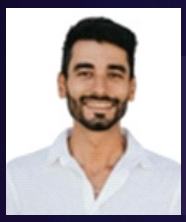
Staff Layout Design Engineer at SYNOPSYS. With 6+ years of experience on custom layout designs for high-speed SerDes IPs in advanced sub-7 nm FinFET and GAA nodes

PROF. PEDRO BARQUINHA

Associate Professor at the Materials Science Department, NOVA FCT and coordinator of the Materials for Electronics, Optoelectronics and Nanotechnology research group (100+ members) at CENIMAT|I3N.

ENG. SIMEON BAMFORD

Neuromorphic engineer and entrepreneur with over 20 years' experience in mixed-signal circuit design. He was CTO of iniVation, commercializing event-based vision sensors. His research spans silicon CMOS neuromorphic systems and flexible electronics, including IGZO and organic TFT technologies.



ENG. MSc. ÃNGELO SANTOS

Currently a PhD candidate at CENIMAT|i3N, NOVA FCT. He is also the electrical characterization laboratory manager at CENIMAT|i3N.

PROGRAM

WEEK1 (26-30 JANUARY 2026):

Advanced layout design on nanoscale planar CMOS technologies: This layout design module focuses on planar CMOS technology and provides a technical introduction to integrated circuit layout fundamentals. It covers transistor construction at layout level, including active, poly, diffusion, contact, and metal layers, as well as key layout considerations for both analog and digital circuits. The course also explores the CADENCE™ full physical design flow, including DRC, LVS, and xRC extraction, with practical exposure to industry-standard layout tools.

WEEK 2 (02-06 FEBRUARY 2026):

Advanced layout design on non-planar finFET CMOS technologies: This layout design module focuses on modern CMOS technologies and provides a technical introduction to integrated circuit layout fundamentals. Emphasis is placed on hands-on design work using the most advanced SYNOPSYS™ IC Design Suite, with practical layout exercises based on non-planar FinFET CMOS technologies using a 16-nm PDK. The module covers transistor construction at the layout level, including active regions, fins, poly, diffusion, contacts, and metal interconnect layers, along with key layout considerations for both analog and digital circuits. In addition, it introduces the complete physical design flow, including DRC, LVS, and xRC extraction, offering practical exposure to industry-standard EDA tools and advanced technology nodes.

WEEK 3 (09-11 FEBRUARY 2026):

Workshop on flexible electronics circuit design: This workshop provides a hands-on introduction to integrated circuit design for flexible electronics, specifically Pragmatic's FlexIC PDK for Cadence. Participants will gain practical experience with device-level circuit schematic simulation and layout using Cadence Virtuoso suite, by implementing a set of small circuits. The course will cover key differences between conventional CMOS and this fascinating new technology, which uses only N-type transistors together with integrated resistors. We will consider variability and performance limits, as well as the morphological freedoms that the technology offers. The course will include a visit to the labs of the Materials Research Center (CENIMAT|i3N) at NOVA FCT, for an introduction to device/circuit fabrication in clean room environment, as well as microscopy and electrical analysis.