When less, means more ...  
... and Moore, the-same!

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The Only Constant is Change ...

- Heraclitus of Ephesus (c.535 - 475 BC)
  Greek philosopher tells us "The only Constant is Change" ...

  ... 22 Centuries later Gordon Moore paraphrases this for the electronic industry!
Moore’s Law

The term Moore's Law was coined by Carver Mead around 1970. Gordon Moore's original statement can be found in his publication "Cramming more components onto integrated circuits", *Electronics Magazine* 19 April 1965:

"The complexity for minimum component costs has increased at a rate of roughly a factor of two per year ... Certainly over the short term this rate can be expected to continue, if not to increase. Over the longer term, the rate of increase is a bit more uncertain, although there is no reason to believe it will not remain nearly constant for at least 10 years. That means by 1975, the number of components per integrated circuit for minimum cost will be 65,000. I believe that such a large circuit can be built on a single wafer."

In 1965 he was experiencing ICs with ~60 transistors ... And basing his observations on ICs with 30 and 15 transistors!

1965: Quad NAND2 = 36 components ...
The VLSI Promise

- Each generation (18mth) gives ...
  - 2x more **Transistors/Chip**
  - 2x Greater Speed
  - 0.5x Lower Power
  - 0.5x Cost
  - A “Shrink Based Evolution Path”

... With Low 2nd Order Costs ...
- Low **FAB** Costs
- Low Mask Cost/Time ...
- Low Silicon Design Cost/Time ...

... has delivered consistently since about 1975

ITRS’99 - Moore’s Law
Previously known-as “Process Node” = ... But from 2005 ITRS stopped using this term!
Design Cost

- Synopsys 2002

### VLSI Challenges

- Each generation still gives more *Transistors/Chip* ...
- But Speed; Power and Cost improvements no-longer great
- Also 2nd Order Effects are becoming 1st Order ...
  - Greater **FAB** Costs
  - Greater Mask Cost/Time ...
    - **DFM** Rules
    - **OPC** and **Checking/Repair**
  - Greater Silicon Design Cost/Time ...
    - More **Productivity** issues
    - More **State Complexity** (**Sq-Law**)
    - More **Non-Functional** issues (eg Power)
  
  ... Also Large Increases in Variability
Systemic Variability (OPC) ... 

... A Cost at Mask-Making
... But also costs at Design and Manufacture

Intrinsic Variability (Atomicity) ...

30 x 30 nm transistor
Time Variability ...

... We cannot rely on the chip staying 100% any more.

Logical Variability ...

- Smaller geometry processes have smaller nodes and shallower junctions, which increase susceptibility to high energy particles ...
- System state-related noise/coupling issues ...
  ... Both lead to ‘random’ logical inconsistency
- Breakdown of Boolean => Physical Mapping
  - Y = A+B ..for.. 99.999...% of the time !!
  - Upsets the entire mathematical basis of Logic Design

... Our HW and SW edifice is built on “100% functional”
A 20Btr Circuit for €15!

- With ~ 65nm Process (~25nm Transistors) ...
  ... There are ~1,000 dead/dying transistors/die (0.1ppm)!

- It ‘works’ because the System Interface is tolerant of errors in the bulk circuit (memory)!

- Failures expected to rise to ~1ppm by 35nm
- ‘Random Logic’ is not tolerant of any defects ...

... So can Failure Rate be low enough for ASIC?

When Moore means Less ...

- Below 100nm ...
  - Transistor Density continues to improve by ~2x every 18mth

... But diminishing returns in the other physical areas ...

  - Speed is not improving
  - Power dissipation is getting worse
  - Leakage is getting worse
  - Defect-Density is getting worse
  - Variability is getting worse
  - Reliability is getting worse
  - FAB and Mask costs are escalating
  - Die-Cost is not reducing (and may be increasing)

... Truly, ‘Silicon’ is facing huge obstacles
... But are they the only huge obstacles being faced?
When Moore Means More-Difficulty ...

Design Complexity and Designer Productivity

Increasing Design Scope ...

... System-Design means more Design Work!
Increased Scope = Increased Work

- Design is now *Concept-to-Product*
- Additional aspects (over traditional Si) include ...
  - IP availability, reliability, integration, legal and cost issues
  - Validation, Verification and Certification
  - Software-in-System (additional design and vulnerability)
  - End-User interface requirements (including aesthetics)
  - Business Issues (eg: TTM, Quality, ...)

System aspects take the Design role beyond ‘Hardware’ ...
... beyond ‘Hardware’ & ‘Software’ ...
... to the abstract realm of Analysis & Refinement

*Thanks to Pink Floyd*
Can’t Make it Right

- Process Variability ...
  - Die/die & Transistor/transistor
  - Atomistic statistics unavoidable
- PPM yields not close enough to zero ...
  - More transistors/die make it worse
  - More contacts and track/die make it worse
- Mask Making
  - Draw features accurately is increasingly improbable
  - Checking => Impossible
- Breakdown of Boolean-Mapping to CMOS Logic

Can’t Test it Right

- Limited test-coverage (Gates/Pin)
- Time and Size of Scan-Test
- Complexity of BIST installation
- Limitations of Functional Test
- Limitations of Speed Test
- Mixed-Signal Test
- The fundamental assumption that “Defects are large” (thus readily visible) breaks down at small geometries
Can't Keep it Right

- Susceptibility to High-energy particles
- Wear-out mechanisms
- State/Time/Age-dependent faults
- Marginality
- State complexity
- Noise and variability

Can't Design it Right

- State-space explosion (Complexity)
- Verification and Validation
- Emergent behaviour
- Modularisation and Reuse
- Methodology
- Software and Hardware
- Increased Design-Scope
- End of ASIC and Scaling
- Power Management (Inc Leakage)
- Increasing Complexity and Quality req’s ...
  ... Yet Reducing Budget, Time and Productivity
Businesses Make Money

- Businesses are Money Making Machines
  - Maximising Profits
  - Maximising Market Value
- For Public Companies, the Executive must consider its Share-Holders interests paramount
  - See Sarbanes-Oxley !!
  - Investors are International
  - Business Decisions are taken on the basis of Optimal Result
  - Returns are made in the Country of Choice
  - Operations are where they are most Economically Delivered
  - International Companies -are- International !

... Charitable companies are (or soon will be) history.

Technology a Means to and End ...

- Though the Technology in these Embedded Computation Products is Awesome ...
  - It is never a primary reason for buying a product
  - Its inclusion or difficulty, never justifies a higher price

... Technology is not the End-Customers main concern.

... But its Quality, Cost and Availability is !
The Changing Product Lifecycle

Cumulative $ Time

Concept
Develop
Introduce
Manufacture
Revenue
Peak
Field EOL

... Development is becoming a major part of a Product's Economy ... And one where optimisation can produce valuable differentiation!

Axes of Evil ... Electronic Tech.

1. Can't Design it Right
2. Can't Make it Right
3. Can't Test it Right
4. Can't Keep it Right
5. Can't Afford it
6. Customers Don't Buy it
Disruption of the Status-Quo ...

Disruptive Technology ...

Improved Technology => Improved Market

Unless ...
- Capability exceeds Need!
- Or Cost exceeds Value

... We have more chip Transistors/chip than many applications can deploy!

“Innovator’s Dilemma”, Christensen
Trifurcation of the Silicon Industry

- Smallest Geometries
  - Only the highest volumes will justify the large costs
  - Lowest transistor-cost
  - Reusable, Configurable, Programmable, Memory devices
  - Increasingly Complex (Non-Boolean) Design
- ~130nm Geometries - Mainstay
  - Applicable for mid-volume applications
  - Lowest die-cost
  - Stable, Secure
  - Boolean Methods and Semi-Custom
  - Bolt-on process modules
  - NV, HV, MEM, etc
  - No shrink route. No more 10%pa price-cut.
- Larger Geometries
  - Applicable to ...
  - High voltage, High Reliability, High Performance Analogue
  - Integration Substrates and Packaging
  - Mixed technology (BiCMOS, etc)
  - Boolean Methods and Semi-Custom

Semi-Custom / ASIC Business Model

- Economic Model...
  - Design is free
  - Masks are cheap
  - FAB is free (utilising spare capacity ... marginal cost only)
- Profitable devices at the next process generation
  - Cost reduction with process scale
- Speed, Power, Performance improvements with shrink
  - All directly linked to Customer Value
- Reliable link between Models and Behaviour
  - Reliable, predictable implementation ... Nothing to wear out
- CMOS is low-power

... All in doubt in 2007!
Design Methodology

- System-Integration density is what matters not greatest logic density
  - RF, Mech, Analogue, Display, IO, etc integration
  - Custom and Semi-Custom for the highest volume applications
  - Packaging (inc external)
- Robustness will emerge as a Design Methodology
  - Necessary to deliver reliable systems on unreliable technology
- Top-down Model Based with bottom-up Reuse will emerge
  - Analysis will be Hierarchical, Asexual and System-down.
  - Implementation (HW, SW, Mech, etc) separated Analysis
  - Reuse in >90% of the design-space is fundamental
- Good-enough is Enough
  - TTM and Cost are vital
  - (Re)Emergence of Standard Product based implementations
  - ‘Software’ based volume product design will (re)emerge
    ... Traditional HW and SW bounds disappear

The Meshing of Business

- Knowledge/Capability/Skills: Enhanced by IT Systems
- Dis-Integration: Enabled by ICT

Any Company!

Manufacturing

Development

Quality

Financial

Marketing

Sales
New-Rules for Business ...

- ICT has made the “Extended and Virtual Enterprise” real
  - We all (Industry, Academia and Nation) operate and compete on the same World Stage
  - No-longer value in obscurity (No more Hiding in the Wings)
    - There is good-money being a Bit-Part Player ...
    - Not every player can be The Star

- The three Elements of 21C business success ...
  1. A Valued Skill or Service (could be very highly valued)
  2. Competitive Productivity Level in it (using IT and other tools).
  3. Efficient Integration within an Extended or Virtual Enterprise (using ICT and supporting Methods).
    - But the Delivered Product (1x2x3) must be World Competitive

... Don’t follow the crowd ... be best at something valuable !

Those who do not learn from the past ...

... are condemned to repeat it!

... So lets remember the foundations of our future ...

George Santayana
Electronics in Telephony (c1965)

GPO Type 706 Telephone

Electronics in Cars (c1975)

Vauxhall Viva HB SL90
The “Fat Mac” (512k) c1980

- 1MIP
- 32bit
- 512k byte memory
- 128kB ROM
- 1.4MB floppy ...
  - System
  - Application
  - And Space!
- Mouse
- 640x480 BW GUI
- Portable!

Has Change Stopped in 21C?

*Very Improbable!*

- I Predict that change will be just as radical over the next, 10, 20, 30 years as it was over the last!

Everything we know and love is in the past ...

... Yet we will spend the rest of our lives in the future
“System Complexity Doubles Every 18mth!”

- Is this what Heraclitus and Moore were trying to say?
Electronic Systems ...

... are not Hardware with a bit of Software!

... They are Functional Alloys of Hw, Sw & Mechanics.

Microelectronic Products

- ID Cards
- Mobile Telephone System
- Security Devices
- Cars
- Entertainment
Software = Hardware = Software

- Logic & State Based Imp’n is not logically partitioned as HW and SW!

Hardware Source?

Software Source?

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Hardware = Software = Hardware

- Both Compiler Outputs are targeted at Implementation Architecture

Hardware? (Verilog Netlist)

Software? (ARM Assembler)

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Example ARM Assembly Language Program AREA

Example, CODE, READONLY; name the code block

ENTRY: marker of first executable instr’n

start: label

MOV r0, #11; put the value 11 in register 0
MOV r1, #31; put the value 31 in register 1
ADD r0, r0, r1; add values in r0 and r1 together

and store total back into r1

STM #11; terminate the program

END: marks the end of the file
System = SW + HW + Mech + Function

(Sub)Systems are alloys of ‘hardware’, ‘software’ and mechanics, delivering End-Product Functionality.

Hardware Module ?  Software Module ?

Design of a System (Or Sub-System)

- A process of Analysis and Information Management ..
- Utilising Appropriate Skills  ... Wherever they are
- Using Structured Methodologies  ... Whichever is appropriate
- And Mapping onto Available Technologies  ... Wherever they can be obtained

… throughout the Product ‘Development’ Process
Analysis .. to.. Implementation

- Concept
- Shelf

- Analysis Languages, Methods & Tools
  - to design reproducible objects comprising...

- Behavioral
  - Mechanical, Electrical, Electronic and Software Implementation Technologies
  - .. cost effectively ..

- Logical
  - Top-Down (Partitioning and Refinement)
  - .. with .. Bottom-Up (Reuse)
  - .. working together to deliver..

- Physical
  - (Sub)System Functionality

Look For ... Standard Architectures

Standard configurable and programmable architecture which is scaleable and may be implemented as Standard Product devices (in a range of ‘sizes’), or implemented within Market Specific integrations

- Cost, TTM and Reuse optimal ...
  - Amortisation of Chip Design Cost through consolidation of volumes
  - Better handling of non-functional infrastructure (power, clock, redundancy, yield, etc)

- Optimisation of Quality

... But a New Design Paradigm (Utilisation)
Look For ... Reparability

Correction of (many) manufacturing errors, and (most) errors that become apparent during use.

- Initial Repair ...
  - Spare rows and columns work for memory
  - Spare cells work for FPGA
- Run-time Repair ...
  - Self-test / reconfigure schemes
  - Spare processors, memory and bus-segments could work for NoC
    - Regular architectures good for this

... But Transient errors need Robustness ...

Look For ... Robustness

Circuits and Software that knows what to do if the requested action Does Not Complete as expected!

- Tolerance of ...
  - Emergent Behaviour (State Complexity, Reuse, etc)
  - Transient Errors (Particles, Noise, etc)
  - Wear-out Errors (Drift, Marginality, Migration, etc)
- Requires a ‘System’ effort ...
  - HW must do what it can ...
    - Check and Report on itself (Local and Regional)
    - Redundancy and FEC schemes
  - SW must do the rest (Regional and Global) ...
    - Read and React to HW error messages
    - Check and Report on itself (Local and Regional)
    - Take appropriate System Corrective actions

... Fail-Functional is the only true Fail-Safe!
Look For ... Micro-Outsourced Process

‘Processes’ compatible with outsourcing smaller and smaller activities to ‘expert providers’ wherever (in the world) they reside.

- Delivering Outsource Value ...
  - Optimise your Core-Value
    - Strive to be best at something that people need
  - Offer your Core-Value efficiently
    - Dominate the market for your Core-Value, by offering your service efficiently to the world ... Don’t let your competition get its nose in!

- Micro-Outsource ...
  - Outsource what is not your Core-Value
    - Don’t do something that others can do more efficiently

... The person competing for your role is not in your country!

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... So Where is Silicon Design?

- In all of them ...
  ...
  just not the primary objective of any of them!
Conclusions

- **System Complexity** will Doubles Every 18mth ... Forever!
  - Silicon-level shrinking will only drive it for a few more years
- Because Si Capacity exceeds our ability to deploy it, the Status-Quo will be disrupted ...
  - Expect major changes in the FAB strategy
  - Expect major changes in the Design Methodology
- Designers are responsible for Whole System (On a chip?)
  - HW, SW, Mechanics, Quality, TTM
  - Working within a Micro-Outsourced International Business Env’t
- Top-down (System) *with* Bottom-up (Reuse)
  - Is the pragmatic approach to Productivity and Quality

... *There is only one past, but an infinite set of futures ...*

“Any sufficiently advanced technology is indistinguishable from magic!”
Arthur C. Clarke